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plication-specific **integrated circuit** (ASIC)]. As new processor architectures are When translating assembly codes from DSPs, it is **common** to encounter highly pipelined software the **subgraph** (CFG). Successive predicates form conjunctions. directed **scheduling** [41]. **ASAP** and ALAP **scheduling** gener- ...
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plexity of silicon-**integrated circuits** proceeds according to For the **CFG** and DFG some **common** basic properties (**ASAP**) driven, in other words, it is the simplest list schedul- execution time instead of rescheduling the task **subgraph**. By ... tended for combined retiming, **scheduling**, and partitioning ...
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